

REMARKS/ARGUMENTS

Favorable reconsideration of this application, as presently amended and in light of the following discussion, is respectfully requested.

Claims 1-7 and 9-29 are presently pending in this application, Claims 9-29 having been withdrawn from further consideration by the Examiner, Claims 1-7 having been amended, and Claim 8 having been canceled by the present amendment.

In the outstanding Office Action, Claims 1-8 were rejected under 35 U.S.C. §103(a) as being obvious over Kanbe et al. (U.S. Patent 6,333,857) in view of EP 1117283 (hereinafter “EP ‘283”).

Claims 1-7 have been amended herein. These amendments are believed to find support in the specification, claims and/or drawings as originally filed, and no new matter is believed to be added thereby. If, however, the Examiner disagrees, the Examiner is invited to telephone the undersigned who will be happy to work in a joint effort to derive mutually satisfactory claim language.

Briefly recapitulating, Claim 1 of the present invention is directed to a multilayer printed wiring board and recites: “a multilayer core substrate comprising a plurality of insulating layers, a front conductive layer formed on a surface of a front outermost one of the insulating layers, a rear conductive layer formed on a surface of a rear outermost one of the insulating layers, a plurality of inner conductive layers formed between the insulating layers, and a plurality of through holes electrically connecting the front, rear and inner conductive layers; an interlayer insulation layer formed over the multilayer core substrate; a conductive layer formed over the interlayer insulation layer and the multilayer core substrate, wherein one of the front and rear conductive layers comprises one of a power source conductive layer and a grounding conductive layer, the other one of the front and rear conductive layers comprises the other one of the power source and grounding conductive layers, the plurality of

inner conductive layers comprises an inner power source conductive layer and an inner grounding conductive layer, the inner power source conductive layer has a thickness which is larger than a thickness of the power source conductive layer, and the inner grounding conductive layer has a thickness which is larger than a thickness of the grounding conductive layer.”

The Office Action states that Kanbe et al. discloses “a multilayer core substrate comprising a plurality of insulating layers, a front conductive layer ..., a rear conductive layer ..., [and] a plurality of inner conductive layers ...” but simply fails to explicitly disclose the thicknesses of the metal layers 101-106. Then, the Office Action concludes that “it would have been obvious ... to form the ... power source layers or the ... grounding layers having thicknesses of which a sum is larger than the thickness of the conductive layer”

However, it is respectfully submitted that Kanbe et al. and EP ‘283 individually or in combination do not teach or suggest “a multilayer core substrate comprising a plurality of insulating layers, a front conductive layer ..., a rear conductive layer ..., a plurality of inner conductive layers formed between the insulating layers ..., wherein one of the front and rear conductive layers comprises one of a power source conductive layer and a grounding conductive layer, the other one of the front and rear conductive layers comprises the other one of the power source and grounding conductive layers, the plurality of inner conductive layers comprises an inner power source conductive layer and an inner grounding conductive layer, the inner power source conductive layer has a thickness which is larger than a thickness of the power source conductive layer, and the inner grounding conductive layer has a thickness which is larger than a thickness of the grounding conductive layer” as recited in amended Claim 1.

More specifically, Kanbe et al. describes that “[t]he composite dielectric layers 111-115 and the metal layers 101-106 constitute a laminated capacitor C1 having 5 dielectric

layers”¹ and that “[t]he exterior metal layers 101 and 106 serve as electrodes of the laminated capacitor C1 and as wiring layers.”² In other words, the metal layers 102-105 are electrodes formed inside the laminated capacitor C1, and as such, it is believed that Kanbe et al. would lead to the *thinner metal layers 102-105* and the *thicker composite dielectric layers 111-115* for larger capacitance,³ thus teaching away from “the inner power source conductive layer has a thickness which is larger than a thickness of the power source conductive layer, and the inner grounding conductive layer has a thickness which is larger than a thickness of the grounding conductive layer.” As discussed in the previous response, EP ‘283 does not disclose a multilayer core substrate but simply shows a core board 3030, lands 3036a formed on the surfaces of the core board 3030 and a plated-through hole 3036 formed *through and across* the core board 3030. It is therefore respectfully submitted that the structure recited in Claim 1 is clearly distinguishable from both Kanbe et al. and EP ‘283 and that their teachings would not render the structure recited in Claim 1 obvious. Applicants respectfully request that the outstanding obviousness rejection based on Kanbe et al. and EP ‘283 be withdrawn.

For the foregoing reason, Claim 1 is believed to be allowable. Furthermore, since Claims 2-7 depend directly or indirectly from Claim 1, substantially the same arguments set forth above also apply to these dependent claims. Hence, Claims 2-7 are believed to be allowable as well.

¹ Kanbe et al., column 16, line 20-23.

² Id, lines 25-27.

³ See, for example, Kanbe et al., column 16, line 65, to column 17, line 7.

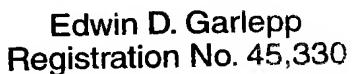
In view of the amendments and discussions presented above, Applicants respectfully submit that the present application is in condition for allowance, and an early action favorable to that effect is earnestly solicited.

Respectfully submitted,

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